IN THE CLAIMS

A complete listing of the pending claims is as follows:

1. (currently amended) An application specific integrated circuit (ASIC) conversion of a programmable logic device (PLD), wherein the programmable logic device comprises a plurality of PLD logic blocks and a PLD routing structure operable to couple logical inputs to each PLD logic block, comprising:

a plurality of ASIC logic blocks corresponding on a one-to-one basis with the plurality of PLD logic blocks; and

an ASIC routing structure configured to couple logical inputs to each ASIC logic block, wherein the coupling provided by the ASIC routing structure is the same as that provided by the PLD routing structure, and wherein the ASIC routing structure is adapted to be delay matched to propagation delays in the PLD routing structure.

2. (original) The ASIC conversion of claim 1, wherein the PLD logic blocks and the ASIC logic blocks are lookup table (LUT)-based logic blocks.

3. (original) The ASIC conversion of claim 1, wherein the PLD logic blocks and the ASIC logic blocks are programmable AND array-based logic blocks.

4. (original) The ASIC conversion of claim 2, wherein the ASIC includes a plurality of metal layers; wherein at least a first metal layer and a second metal layer in the plurality are coupled by vias each selected so as to provide either a logic high or a logic low value to the plurality of ASIC logic blocks to provide the same truth tables as used in the PLD logic blocks.

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5. (original) The ASIC conversion of claim 2, wherein the ASIC includes at least one metal layer, wherein traces formed in the metal layer are customized to provide the same truth tables for the ASIC logic blocks as are used in the PLD logic blocks.

6. (original) The ASIC conversion of claim 4, wherein only the first and second metal layers are coupled by vias selected so as to provide either a logic high or a logic low value to the plurality of ASIC logic blocks to thereby provide the same truth tables as in the PLD logic blocks.

7. (original) The ASIC conversion of claim 4, wherein the first metal layer includes traces carrying voltage levels VCC and VSS, and wherein the vias are selected to couple to VCC to provide a logic high value and to couple to VSS to provide a logic low value.

8. (original) The ASIC conversion of claim 1, wherein the ASIC includes a plurality of metal layers, and wherein at least a first metal layer and a second metal layer in the plurality are coupled by vias each selected so that the coupling provided by the ASIC routing structure routing structure is the same as that provided by the PLD routing structure.

9. (original) The ASIC conversion of claim 8, wherein the PLD routing structure is a buffered, segmented routing structure, each buffered PLD routing segment corresponding to an ASIC buffered routing segment, and wherein the vias are each selected so that the coupling provided by the ASIC routing structure is the same as that provided by the PLD routing structure on a segment-by-segment basis.

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10. (currently amended) The ASIC conversion of claim 9, ~~wherein each PLD routing segment couples to other routing segments that may select for inputs other than the PLD routing segment so as to affect the propagation speed in the PLD routing segment, and~~

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wherein the adaptation of the ASIC routing structure to be delay matched comprises, for each ASIC routing segment, ~~may be coupled to~~ a diode load coupled through a via provided between the first and second metal layer to match the ~~affected~~ propagation ~~speed~~ delay in the corresponding PLD routing segment.

11. (currently amended) The ASIC conversion of claim 9, wherein the buffers in each PLD routing segment ~~may each be~~ are constructed with transistors having one of a plurality of channel widths, the selected channel width affecting the propagation delay through the buffer, and wherein the adaptation of the ASIC routing structure to be delay matched comprises ~~each buffer in each ASIC routing segment is~~ a plurality of programmable ~~buffer~~ buffers, each programmable buffer operable to match the propagation delay in ~~the~~ a corresponding buffer in the PLD routing structure.

12. (original) The ASIC conversion of claim 11, wherein each programmable buffer comprises a plurality of inverters operable to be selectively coupled in parallel.

13. (original) The ASIC conversion of claim 12, wherein the plurality of inverters comprises three inverters.

14. (withdrawn) A method of ASIC conversion of a programmable logic device (PLD), the PLD being configured to perform a desired task, wherein the programmable logic device comprises a plurality of lookup-table (LUT)-based PLD logic blocks coupled together by a PLD routing structure, the method comprising:

configuring a mask for at least one via layer of an ASIC device, wherein the ASIC device will include a plurality of LUT-based ASIC logic blocks corresponding on a one-to-one basis with the plurality of LUT-based PLD logic blocks and an ASIC routing structure configured to couple logical inputs to each ASIC logic block and to couple logical outputs from each ASIC logic block, wherein the mask configuring act configures the mask such that

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each via will provide either a logic high or a logic low value to the plurality of ASIC logic blocks to thereby provide the same truth tables as used in the PLD logic blocks; and

manufacturing the ASIC using the configured mask.

15. (withdrawn) The method of ASIC conversion of claim 13, wherein the mask configuring act comprises selecting each via to either couple to a logic high value or to a logic low value so as to thereby provide the same truth tables as used in the PLD logic blocks.

16. (withdrawn) The method of claim 13, further comprising:

powering the manufactured ASIC, the powered ASIC thereby performing the desired task.

17. (currently amended) An application specific integrated circuit (ASIC) conversion of a programmable logic device (PLD), wherein the programmable logic device comprises a plurality of PLD logic blocks configured to perform a desired task and a PLD routing structure operable to couple logical inputs to each PLD logic block, comprising:

a plurality of ASIC logic blocks corresponding on a one-to-one basis with the plurality of PLD logic blocks;

an ASIC routing structure configured to couple logical inputs to each ASIC logic block, wherein the coupling provided by the ASIC routing structure is the same as that provided by the PLD routing structure, and wherein the ASIC routing structure is adapted to be delay matched to propagation delays in the PLD routing structure; and

means for configuring the plurality of ASIC logic blocks to perform the desired task.

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18. (original) The ASIC conversion of claim 17, wherein the ASIC includes a plurality of metal layers, and wherein the means for configuring the plurality of ASIC logic blocks includes a plurality of vias between at least a first metal layer and a second metal layer, each

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via being positioned so as to provide either a logic high or a logic low value to an ASIC logic block, the plurality of vias thereby supplying the same truth tables as used in the PLD logic blocks.

19. (original) The ASIC conversion of claim 17, wherein the means for configuring the plurality of ASIC logic blocks includes a plurality of conductors within at least one metal layer of the ASIC, each conductor being positioned so as to provide either a logic high or a logic low value to an ASIC logic block, the plurality of conductors thereby supplying the same truth tables as used in the PLD logic blocks.

20. (original) The ASIC conversion of claim 18, wherein the routing structure in the programmable logic device is a buffered, segmented routing structure, each buffered PLD routing segment corresponding to an ASIC buffered routing segment.

21. (withdrawn) A method of implementing a design in an application specific integrated circuit (ASIC), wherein the design was first implemented in a programmable logic device (PLD) having a plurality of programmable logic blocks and a programmable routing structure, the method comprising:

providing in the ASIC a plurality of logic blocks corresponding to the programmable logic blocks of the PLD;

providing in the ASIC a routing structure corresponding to the programmable routing structure of the PLD; and

forming permanent connections in the ASIC routing structure to produce a signal propagation delay in the ASIC routing structure that matches substantially the signal propagation delay in the corresponding PLD programmable routing structure.

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22. (withdrawn) The method of claim 21, wherein forming permanent connections in the ASIC routing structure comprises selectively forming vias between conductive layers to provide a desired route through the routing structure.

23. (withdrawn) The method of claim 21, wherein forming permanent connections in the ASIC routing structure comprises selectively forming vias between conductive layers to produce a desired capacitive load on the routing structure.

24. (withdrawn) The method of claim 23, wherein the desired capacitive load is provided by a programmable diode formed in a conductive layer.

25. (withdrawn) The method of claim 21 including providing a programmable buffer in the routing structure, wherein forming permanent connections in the ASIC routing structure comprises permanently programming the buffer to provide a desired signal propagation delay through the buffer.

26. (withdrawn) The method of claim 25, wherein the programmable buffer comprises a plurality of programmable inverters arranged in parallel.

27. (withdrawn) The method of claim 21 including forming permanent connections in the ASIC logic blocks that correspond to programmable connections formed in the PLD programmable logic blocks;

28. (withdrawn) The method of claim 27, wherein forming permanent connections in the ASIC logic blocks comprises selectively forming vias between conductive layers to provide a desired functionality for the block.

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29. (withdrawn) The method of claim 28, wherein one of the conductive layers contains separate traces, and a vias is formed between a trace and another conductive layer.

30. (withdrawn) The method of claim 27, wherein forming permanent connections in the ASIC logic blocks comprises selectively coupling conductive traces to vias to provide a desired functionality for the block.

31. (withdrawn) The method of claim 30, wherein the conductive traces are contained in one conductive layer.

32. (original) An application specific integrated circuit (ASIC) comprising:

a plurality of logic blocks corresponding to programmable logic blocks of a programmable logic device (PLD); and

a routing structure corresponding to the programmable routing structure of the PLD but having permanently formed connections therein, the ASIC routing structure adapted to produce a signal propagation delay that matches substantially the signal propagation delay in the corresponding PLD programmable routing structure.

33. (original) The ASIC of claim 32, wherein the permanently formed connections of the ASIC routing structure include selectively formed vias between conductive layers to provide a desired route through the routing structure.

34. (original) The ASIC of claim 32, wherein the permanently formed connections of the ASIC routing structure include selectively formed vias between conductive layers to produce a desired capacitive load on the routing structure

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35. (original) The ASIC of claim 34, wherein the desired capacitive load is provided by a programmable diode formed in a conductive layer.

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36. (original) The ASIC of claim 32, wherein the permanently formed connections of the ASIC routing structure include a buffer permanently programmable to provide a desired signal propagation delay through the buffer.

37. (original) The ASIC of claim 36, wherein the programmable buffer comprises a plurality of programmable inverters arranged in parallel.

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